Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	34	(AMATANGELO-MATTHEW-J KHWAJA-ZAKARIA LEVY-HOWARD LEVY-HOWARD-L LEVY-HOWARD-LAWRENCE LEVY-HOWARD-M LEVY-HOWARD-S PAREDES-JOSE PAREDES-JOSE-A PAREDES-JOSE-ANGEL PATEL-BINTA-M PATEL-BINTA-MINESH).in.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/12 20:51
S2	30	S1 and (timing or time)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/12 20:52
S3	21	S2 and ((timing or time) with (element or circuit or block))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/12 21:03
S4	2	S2 and ((timing or time) with (element or circuit or block) with determin$4)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/12 21:14
S5	82501	((timing or time) with (element or circuit or block) with determin$4)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/12 21:14
S6	39	timing adj determin$5 adj block	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/12 21:15
S7	1	S6 and (static with timing)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/12 21:18
S8	5	("6021261" "5651012" "5790830" "6083273" "6158022").pn.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/12 21:28
S9	57	(worst same case same timing same path) and (best same case same timing same path)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/12 21:30
S10	35	S9 and circuit same (simulat$5 or emulat$5 or model$5)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/12 21:30
S11	32	S9 and element	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/12 21:31

S12	22	S9 and ((element or circuit or block) with set)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/12 21:31

"512" Search Results

	Document ID	Issue Date	Title	Current OR	Current XRef
1	US 20040221252 A1	20041104	METHOD FOR STATIC TIMING VERIFICATION OF INTEGRATED CIRCUITS HAVING VOLTAGE ISLANDS	716/6	
2	US 20040113668 A1	20040617	Integrated circuit timing debug apparatus and method	327/158	
3	US 20040100286 A1	20040527	Modeling miller effect in static timing analysis	324/677	
4	US 20030182098 A1	20030925	Derating factor determination for integrated circuit logic design tools	703/19	
5	US 20030009318 A1	20030109	Method of utilizing timing models to provide data for static timing analysis of electronic circuits	703/19	
6	US 20020116674 A1	20020822	Boundary scan delay chain for cross-chip delay measurement	714/724	
7	US 6791343 B2	20040914	Modeling miller effect in static timing analysis	324/677	324/609; 324/617; 324/628; 324/76.11; 702/65; 716/2
8	US 6665847 B1	20031216	Accurate and realistic corner characterization of standard cells	716/5	347/9
9	US 6487701 B1	20021126	System and method for AC performance tuning by thereshold voltage shifting in tubbed semiconductor technology	716/4	716/5; 716/6
10	US 6442741 B1	20020827	Method of automatically generating schematic and waveform diagrams for analysis of timing margins and signal skews of relevant logic cells using input signal predictors and transition times	716/6	702/118; 702/125; 702/67; 702/73; 702/79; 703/15

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11	US 6430731 B1	20020806	Methods and apparatus for performing slew dependent signal bounding for signal timing analysis	716/6	716/4; 716/5
12	US 6286126 B1	20010904	Methods, apparatus and computer program products for performing post-layout verification of microelectronic circuits using best and worst case delay models for nets therein	716/6	
13	US 6272668 B1	20010807	Method for cell swapping to improve pre-layout to post-layout timing	716/10	716/12; 716/2; 716/6; 716/9
14	US 6185706 B1	20010206	Performance monitoring circuitry for integrated circuits	714/724	716/4; 716/5
15	US 6124143 A	20000926	Process monitor circuitry for integrated circuits	438/18	324/713; 327/35; 327/378; 438/11; 702/65
16	US 5896300 A	19990420	Methods, apparatus and computer program products for performing post-layout verification of microelectronic circuits by filtering timing error bounds for layout critical nets	716/10	703/15; 716/5; 716/6
17	US 5859986 A	19990112	Bandwidth efficient method and means for resynchronizing a master and slave over a clocked, arbitrated, bidirectional multistate parallel bus using local data recirculation, wait states, and cycle stealing	713/401	713/375

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18	US 5619418 A	19970408	Logic gate size optimization process for an integrated circuit whereby circuit speed is improved while circuit area is optimized	716/6	
19	US 5396435 A	19950307	Automated circuit design system and method for reducing critical path delay times	716/6	703/19; 716/18
20	US 5180937 A	19930119	Delay compensator and monitor circuit having timing generator and sequencer	327/276	
21	US 4433252 A	19840221	Input signal responsive pulse generating and biasing circuit for integrated circuits	327/262	327/394; 327/538; 327/543; 365/233
22	NN86044981	19860401	Timing-Influenced Layout Design		

Terms used **worst case timing path best case element** OR **circuit** OR **block** OR **component** AND **set**

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1 Managing power and performance for System-on-Chip designs using Voltage Islands

David E. Lackey, Paul S. Zuchowski, Thomas R. Bednar, Douglas W. Stout, Scott W. Gould, John M. Cohn

November 2002 **Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(96.51 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper discusses Voltage Islands, a system architecture and chip implementation methodology, that can be used to dramatically reduce active and static power consumption for System-on-Chip (SoC) designs. As technology scales for increased circuit density and performance, the need to reduce power consumption increases in significance as designers strive to utilize the advancing silicon capabilities. The consumer product market further drives the need to minimize chip power consumption.Effectiv ...

2 Automating RT-level operand isolation to minimize power consumption in datapaths

M. Münch, B. Wurth, R. Mehra, J. Sproch, N. Wehn

January 2000 **Proceedings of the conference on Design, automation and test in Europe**

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1 **Testing embedded cores using partial isolation rings**
Touba, N.A.; Pouya, B.;
VLSI Test Symposium, 1997., 15th IEEE , 27 April-1 May 1997
Pages:10 - 16

[Abstract] [PDF Full-Text (676 KB)] IEEE CNF

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2 **False timing path identification using ATPG techniques and delay-ba information**
Jing Zeng; Abadir, M.; Abraham, J.;
Design Automation Conference, 2002. Proceedings. 39th , 10-14 June 2002
Pages:562 - 565

[Abstract] [PDF Full-Text (515 KB)] IEEE CNF

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3 **Have I really met timing? - validating primetime timing reports with SPICE**
Thiel, T.;
Design, Automation and Test in Europe Conference and Exhibition, 2004. Proceedings , Volume: 3 , 16-20 Feb. 2004
Pages:114 - 119 Vol.3

[Abstract] [PDF Full-Text (263 KB)] IEEE CNF

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4 **Modifying user-defined logic for test access to embedded cores**
Pouya, B.; Touba, N.A.;
Test Conference, 1997. Proceedings., International , 1-6 Nov. 1997
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